

1   1.   A method of connecting an integrated circuit die to a substrate,  
2   comprising:

3           identifying a block of circuitry to be disabled within the integrated circuit  
4   die;

5           applying a pattern of solder bumps to one of the die and the substrate,  
6   the pattern of solder bumps excluding at least one solder bump used for  
7   connection to the block of circuitry;

8           placing the integrated circuit die on the substrate with solder pads on  
9   the die aligned with corresponding solder pads on the substrate and with the  
10   pattern of solder bumps disposed between the die and the substrate; and  
11           heating the solder bumps to cause the solder to flow and form electrical  
12   connections between the substrate and the die.

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14   2.   The method according to claim 1, wherein the excluded solder bump, if  
15   present, would convey power supply voltage to the block of circuitry.

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17   3.   The method in accordance with claim 1, wherein the applying is carried  
18   out by applying solder through a mask selected in accordance with the block  
19   of circuitry to be disabled.

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21   4.   The method according to claim 1, wherein the identifying is carried out  
22   by testing blocks of circuitry for functionality, and wherein the block of circuitry  
23   to be disabled is determined to not be functional.

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2 5. The method according to claim 1, wherein the identifying is carried out  
3 by determining that a specified performance criterion is required.

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5 6. The method according to claim 1, wherein the block of circuitry to be  
6 disabled comprises one of a plurality of microprocessor cores.

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8 7. The method according to claim 1, wherein the block of circuitry to be  
9 disabled comprises one of a plurality of memory blocks.

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11 8. The method according to claim 1, wherein the block of circuitry to be  
12 disabled comprises one of a plurality of redundant blocks of circuitry.

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14 9. The method according to claim 1, wherein the applying further  
15 comprises, applying a solder bump used to connect ground to the block of  
16 circuitry to be disabled.

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1 10. A method of applying solder bumps for soldering a substrate to an  
2 integrated circuit die, comprising:

3 identifying a block of circuitry on the integrated circuit die that is to be  
4 disabled; and

5 applying a pattern of solder bumps to one of the die and the substrate,  
6 the pattern of solder bumps excluding at least one solder bump used for  
7 connection to the block of circuitry that is to be disabled.

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9 11. The method according to claim 10, wherein the excluded solder bump,  
10 if present, would convey power supply voltage to the block of circuitry.

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12 12. The method in accordance with claim 10, wherein the applying is  
13 carried out by applying solder through a mask selected in accordance with the  
14 block of circuitry to be disabled.

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16 13. The method according to claim 10, wherein the identifying is carried out  
17 by testing blocks of circuitry for functionality, and wherein the block of circuitry  
18 to be disabled is determined to not be functional.

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20 14. The method according to claim 10, wherein the identifying is carried out  
21 by determining that a specified performance criterion is required.

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23 15. The method according to claim 10, wherein the block of circuitry to be

1 disabled comprises one of a plurality of microprocessor cores.

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3 16. The method according to claim 10, wherein the block of circuitry to be  
4 disabled comprises one of a plurality of memory blocks.

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6 17. The method according to claim 10, wherein the block of circuitry to be  
7 disabled comprises one of a plurality of redundant blocks of circuitry.

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9 18. The method according to claim 10, wherein the applying further  
10 comprises, applying a solder bump used to connect ground to the block of  
11 circuitry to be disabled.

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1 19. A method of configuring functionality of an integrated circuit die,  
2 comprising:

3 identifying a block of circuitry to be configured by selectively making an  
4 electrical connection between a substrate and the integrated circuit die;

5 applying a pattern of solder bumps to one of the die and the substrate,  
6 the pattern of solder bumps selectively excluding at least one solder bump  
7 used for connection to the block of circuitry;

8 placing the integrated circuit die on the substrate with solder pads on  
9 the die aligned with solder pads on the substrate and the pattern of solder  
10 bumps disposed therebetween; and

11 heating the solder bumps to cause the solder to flow and form electrical  
12 connections between the substrate and the die.

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14 20. The method according to claim 19, wherein the excluded solder bump,  
15 if present, would convey power supply voltage to the block of circuitry.

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17 21. The method according to claim 19, wherein the excluded solder bump,  
18 if present, would convey a signal as an input to a logic circuit in the block of  
19 circuitry.

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21 22. The method in accordance with claim 19, wherein the applying is  
22 carried out by applying solder through a mask selected in accordance with the  
23 block of circuitry to be disabled.

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1    23. An integrated circuit device, comprising:  
2                an integrated circuit die having a plurality of solder pads used for  
3        conveying signals to and from the die, the integrated circuit having a plurality  
4        of blocks of circuitry;  
5                a substrate having a plurality of solder pads corresponding to at least a  
6        portion of the integrated circuit die's solder pads;  
7                a plurality of solder bumps connecting the substrate to the integrated  
8        circuit die; and  
9                wherein at least one of the blocks of circuitry is configured by virtue of  
10      omission of a solder bump for at least one connection between the substrate  
11      and the at least one of the plurality of blocks of circuitry.

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13    24. The apparatus according to claim 23, wherein the one of the plurality of  
14      blocks of circuitry is disabled by omission of a solder bump that supplies  
15      power supply voltage to the at least one of the block of circuitry.

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17    25. The apparatus according to claim 24, wherein the block of circuitry that  
18      is disabled is identified by testing the plurality of blocks of circuitry for  
19      functionality.

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21    26. The apparatus according to claim 24, wherein the block of circuitry that  
22      is disabled is determined to not be functional by said testing.

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1    27. The apparatus according to claim 24, wherein the block of circuitry that  
2    is disabled comprises one of a plurality of microprocessor cores.

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4    28. The apparatus according to claim 24, wherein the block of circuitry that  
5    is disabled comprises at least one of a plurality of memory blocks.

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7    29. The apparatus according to claim 24, wherein the block of circuitry that  
8    is disabled comprises one of a plurality of redundant blocks of circuitry.

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10   30. The apparatus according to claim 24, wherein one of the plurality of  
11   solder bumps connects the substrate to a ground node in the block of circuitry  
12   that is disabled.

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14   31. The apparatus according to claim 23, wherein the omitted solder bump,  
15   if present, would connect the substrate to a logic input forming a part of the  
16   block of circuitry.

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18   32. The apparatus according to claim 23, wherein the substrate forms part  
19   of a chip carrier.

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21   33. The apparatus according to claim 23, wherein the one of the plurality of  
22   blocks of circuitry is configured by selective connection of a signal to a logic  
23   gate.

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